In the Specification:

Please amend Paragraph 00010 as set forth below:

During the IPO process, a method in accordance with the present invention helps solve various types of problems: long run-time for each run, increased layout area, increased congestion, insignificant timing improvement, and a long design period caused by the previous problems. The invention solves above problems by employing the concept of "timing violation potential," to aid in the selection components or nets (interconnects) or both with the largest violation potential by using user input criteria and then running an IPO only for the selected components or nets. Although a timing analyzer reports critical paths, not everything in the critical path can get the same amount of improvement. Some components or nets have a greater potential to improve timing than others. The concept of "timing violation potential" is used to characterize each component or net (interconnect). If the component or net has a larger timing violation potential, then it can cause larger timing violations, and if these are operated on first, it is more likely to result in the largest timing improvement. For the rest of the components or nets, even if they are still in critical path, operating on them may not achieve any more timing improvement[of timing], so these nets are removed from the critical component or nets list of the critical path. Clock nets sometimes cause very big transition and cap violations, but they are solved by clock tree synthesis, so the clock nets are removed from consideration. After dealing with the components or nets with the largest timing violation potential, the Worst Negative Slack (WNS) of critical path is greatly reduced, and in the mean time, the critical path, which may have only small timing violations, may have received enough timing improvement to become a non-critical path. So this selective IPO will also reduce total number of critical paths as well as Total Negative Slack (TNS) of the design. Because less than 10% of all components or nets (or both) in the critical path are operated on, there is a run-time and memory usage advantage. For the same reason, the IPO tool does not have to size up too many cells, and does not have to insert too many buffer or inverters or split too many nodes to get the same amount of timing improvement, so the selective IPO approach has a smaller increase in circuit area, and a smaller congestion problem after IPO. In high density UDSM physical design, this approach achieves faster timing closure and better timing improvements.